

REMARKS

The application contains claims 3-7, 9-12, 17-20, 23, and 25-26. By this amendment, claims 1, 21, and 22 have been canceled. In view of the foregoing amendments and following remarks, Applicants respectfully request allowance of the application.

CLAIM OBJECTIONS

Applicants believe that the foregoing amendments overcome the claim objections noted in paragraphs 3-7 of the office action.

PRIOR ART REJECTIONS

All pending claims stand rejected based on prior art. Applicants respectfully request withdrawal of these outstanding rejections because the prior art does not disclose, teach, or suggest all elements of the pending claims.

Claims 4-6 are allowable over the cited art.

Claim 4 stands rejected as obvious over Pickett (U.S. Patent No. 5,968,169) and Hennessy. Claim 4 recites in part:

determining, with reference to other instructions read previously from the instruction pipestage, whether immediate processing of the call instruction would exceed a predetermined access rate of the instruction pipe to a return-stack buffer and,

stalling processing of the call instruction until sufficient time has expired to synchronize processing of the call instruction with the predetermined access rate.

Both Pickett and Hennessy fail to disclose, teach, or suggest stalling processing of the call instruction to synchronize processing of the call instruction with the predetermined access rate. In Pickett, only one pipeline is accessing the return stack buffer, and thus, Pickett's pipeline has an access rate of 100% to a return stack buffer. Therefore, there is no need in Pickett to synchronize processing of the call instruction with the predetermined access rate.

Hennessy does not cure this deficiency of Pickett. Hennessy discloses the various structural hazards in the context of a general system memory, but they do not involve a return

stack buffer. The Examiner alleges that it would be obvious to modify Pickett's system to accommodate for Hennessy's structural hazards, which is caused in the context of general system memory. To provide motivation or suggestion to combine, the Examiner alleges the following:

A call instruction results in an address being pushed on the stack. If two calls instructions are executed at the same time, then two pushes to the stack will need to be performed at the same time. However, this is not possible with a stack, the only place to write is at the top of the stack. And, if both calls are allowed to write to the top of the stack, one of the values will be overwritten. Therefore, if immediate processing of a call instruction would exceed a predetermined access rate to a return stack buffer, then the call instruction must be stalled until sufficient time has expired. This will ensure that both calls are executed correctly. As a result, in order to ensure correct execution, it would have been obvious to [combine Pickett and Hennessy.]

To reject a claim as obvious, the Examiner has a burden to prove that there is some motivation or suggestion, at the time of the invention, to combine the prior art. Here, neither Pickett nor Hennessy mentions anything about two call instructions competing for the same location with the return stack buffer, anything about a call instruction with a predetermined access rate to a return stack buffer, or any of these events alleged by the Examiner. Aside from personal speculation, the Examiner has not provided any evidence to prove motivation or suggestion for the alleged combination. Rather, the Examiner relies solely on his hindsight reconstruction of the prior art to manufacture the alleged motivation to combine the cited art, which is wholly improper. Accordingly, the obviousness rejection to claim 4 must be withdrawn. Claims 5-6, which depend from independent claim 4, also define over the cited art.

Claims 7 and 9 are allowable over the cited art.

Claims 7 and 9 stand rejected as obvious over Hennessy and Hoyt (U.S. Patent No. 5,604,877). Applicants respectfully request reconsideration because the cited art does not teach or suggest each and every element of these claims. Claim 7 recites in part:

determining, with reference to other instructions read previously from the instruction pipestage, whether immediate processing of the call instruction would exceed the instruction pipe's access allocation to an external resource.

None of the cited art discloses, teaches, or suggests determining whether immediate processing of the call instruction would exceed the instruction pipe's access allocation to an external resource. In Hoyt, only one pipeline is accessing a return stack buffer, and thus, Hoyt's pipe

has a 100% access rate to the return stack buffer. Thus, there is no need to allocate the instruction pipe's access to the external source. Further, there is no need to determine whether immediate processing of the call instruction would exceed the instruction pipe's access allocation to the external resource. Hennessy fails to cure the deficiency of Hoyt because Hennessy's various structural hazards do not involve call instructions. Thus, the alleged combination of Hennessy and Hoyt fails to render claim 7 obvious. Accordingly, claims 7 and 9 define over the art.

Claims 10-12 are allowable over the prior art.

Claims 10-12 stand rejected as anticipated by IBM. Claim 10 recites in part:

determining, with reference to other instructions read previously from the instruction pipestage, whether a return address is available to the instruction pipe prior to expiration of the round-trip communication latency period with the return-stack buffer.

IBM does not teach or suggest this claimed feature. In particular, IBM does not look to the instruction pipe for the return address. Instead, IBM searches for a return address in the internal return stack buffer, not in the instruction pipe. Moreover, IBM does not even mention the round-trip communication latency period at all. Rather, IBM determines the execution time of a call instruction, or the amount time it takes to execute a call instruction. Thus, IBM fails to disclose, teach, or suggest determining, with reference to other instructions read previously from the instruction pipestage, whether a return address is available to the instruction pipe prior to expiration of the round-trip communication latency period with the return-stack buffer. Accordingly, the anticipation rejection of independent claim 10 should be withdrawn. Claims 11-12, which depend from claim 10, also define over the art.

Claims 17-20 are allowable over the prior art.

Claims 17-20 stand rejected as obvious over Pickett and Sproch et al. (U.S. Patent No. 6,247,134). Claim 17 recites:

a first instruction pipe, comprising:
 a first plurality of cascaded pipestages, and
 a return stack buffer provided in communication with at least one of the first pipestages, and

a second instruction pipe, comprising:

a second plurality of cascaded pipestages, at least one of the second plurality of pipestages provided in communication with the return stack buffer.

Pickett does not disclose multiple pipes, but rather, one pipeline having six stages. Moreover, Pickett fails to disclose, teach, or suggest a return stack buffer that is included in a first instruction pipe and also in communication with a second instruction pipe. Additionally, Sproch fails to overcome the deficiency of Pickett because Sproch's system only includes one pipeline. Thus, independent claim 17 is patentable over the cited art. Accordingly, claims 18-20, which depend from claim 17, are also patentable over the art.

Claim 23 is allowable over the prior art.

Claim 23 stands rejected as anticipated by Hoyt. Claim 24 stands rejected as obvious over Hoyt and IBM. Claim 23 has been amended to recite:

responsive to a return instruction in a first pipestage of an instruction pipe:

determining whether the pipestage processed a prior return instruction faster than a latency period for round trip communication between the pipestage and the return stack buffer,

if so, stalling the downstream pipestages until the period for processing a prior return instruction equals the round trip communication latency period

As indicated by the Examiner, Hoyt does not teach this subject matter. IBM fails to cure the deficiency of Hoyt. IBM discloses that "if a return is followed by another return instruction **before the first one completes**, you need to hold the second return in decode until the first one completes in write back stage." This "before the first one completes" refers to execution time of a return instruction (or the time it takes to execute a return instruction), but not the round-trip communication latency period with the return stack buffer. Thus, IBM fails to disclose, teach, or suggest stalling the pipestages until the period for processing a prior return instruction equals the round trip communication latency period. Hoyt also mentions nothing about the round-trip communication latency period. Thus, even the alleged combination of these two references falls short of disclosing this claimed feature. Accordingly, claim 23 defines over the art.

Claims 25-26 are allowable over the prior art.

Claims 25-26 stand rejected as obvious over Hoyt and Cosgrove et al. (U.S. Patent No. 4,399,507). Claim 25 recites in part:

a pair of registers provided between first and second pipestages of the plurality,

a first of the registers to store a return address received from the first pipestage during receipt of a call instruction,

a second of the registers to store a return address received from a return stack buffer.

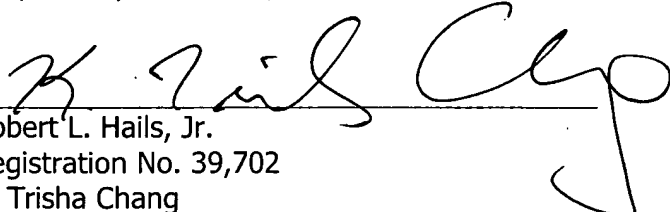
Neither Hoyt nor Cosgrove disclose, teach, or suggest a pair of local storage devices, one receiving a return instruction from within the instruction pipe and the other receiving an instruction from a return stack buffer. The Examiner alleges that it would be obvious to modify Hoyt to include a second register as taught by Cosgrove to allow quick address access for a next instruction. The Examiner's assertion is based on Hoyt's disclosure of a register, which stores a return address received from an instruction pipe and Cosgrove's disclosure of a register, which stores a return address received from a return stack buffer. But, there is nothing in Hoyt or Cosgrove that provides any suggestion or motivation to combine these two registers. In fact, both Hoyt and Cosgrove disclose a system with only one register. Further, the Examiner fails to give any plausible reason or cite any reference that would motivate or even suggest to one skilled in the art at the time of the invention to combine Hoyt and Cosgrove to include two registers; one to store a return address from a return stack buffer and the other to store a return address from an instruction pipe, as claimed in claim 25. Again, the references themselves or some other teaching must provide some suggestion or motivation to combine their teachings. The Examiner may not conclude that Applicants' invention is obvious based on improper hindsight reasoning. Accordingly, claim 25 and its dependent claim 26 define over the art.

CONCLUSION

In view of the above amendments and remarks, Applicants respectfully submit that the present application is now in condition for allowance. A timely Notice to that effect is earnestly solicited. The Examiner is invited to contact the undersigned at (202) 220-4200 to discuss any aspect of the application.

Respectfully submitted,

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